

Design of All Passive Blocker-Tolerant Reconfigurable RF Front-end Filter

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Abstract—This paper presents a tunable active bandpass filter with adjustable notch close to the passband for blocker rejection. The proposed filter is based on two-path signal cancellation and consists of a top-C coupled tunable bandpass filter in parallel with an inductor. The proposed filter is implemented with high-Q N-path filter/resonator blocks in 65-nm CMOS process. The passband of the filter is tunable from 0.4 GHz to 2.2 GHz with a 3-dB bandwidth of 14.4–15.6 MHz, an insertion loss of 3.6–5.8 dB, a noise figure of 3.8–6 dB, and a total power consumption of 12.4–42 mW. Transmission zero is created close to the passband with a minimal offset of 40 MHz and are tunable across a 25 MHz range with up to 54 dB rejection. The blocker 1-dB compression point is 8.5 dBm and the out-of-band IIP3 is 23.5 dBm. The proposed filter provides a promising solution to multi-standard, multi-frequency software-defined radio applications.

I. INTRODUCTION

Utilizing two or more adjacent or non-adjacent RF channels is proposed in the long-term evolution (LTE)-advanced standard to meet the growing demand of high data rate wireless communications. Simultaneous reception of multiple carriers called "Carrier Aggregation", are supported in release 11 of 3GPP LTE standard [1]. Carrier aggregation (CA) requires the receiver to pick up weak desired signals from multiple RF channels and significantly reject all the unwanted ones. Both intra-band aggregation (RF channels belong to the same band) and inter-band aggregation (different bands) are supported in 3GPP standard. The channels can be adjacent to one another (contiguous) or not (non-contiguous) for intra-band aggregation which poses new RF design challenges. For inter-band CA, it is natural to increase the number of receivers corresponding to the number of simultaneous carriers with a direct area and power penalty. As the frequency separation is small, the synthesizers must avoid injection pulling which requires complex frequency plan. On the other hand, LTE allows different bandwidths for two channels if part of the spectrum is already occupied by another user to maximize spectral usage. That user's signal can be much stronger than the desired one at the receiver input which acts like as a blocker. Suppressing that high power blocker significantly is necessary to avoid desensitizing the receiver.

Several architectures have been proposed to handle large blockers. A combination of bandpass and band-reject filtering is independently proposed in [2], [3] to suppress blockers. Due to the insertion of bandstop filter/resonator between bandpass filter/resonators in [2], the passband is affected when the notch frequency is close to the passband. On the other hand, the front

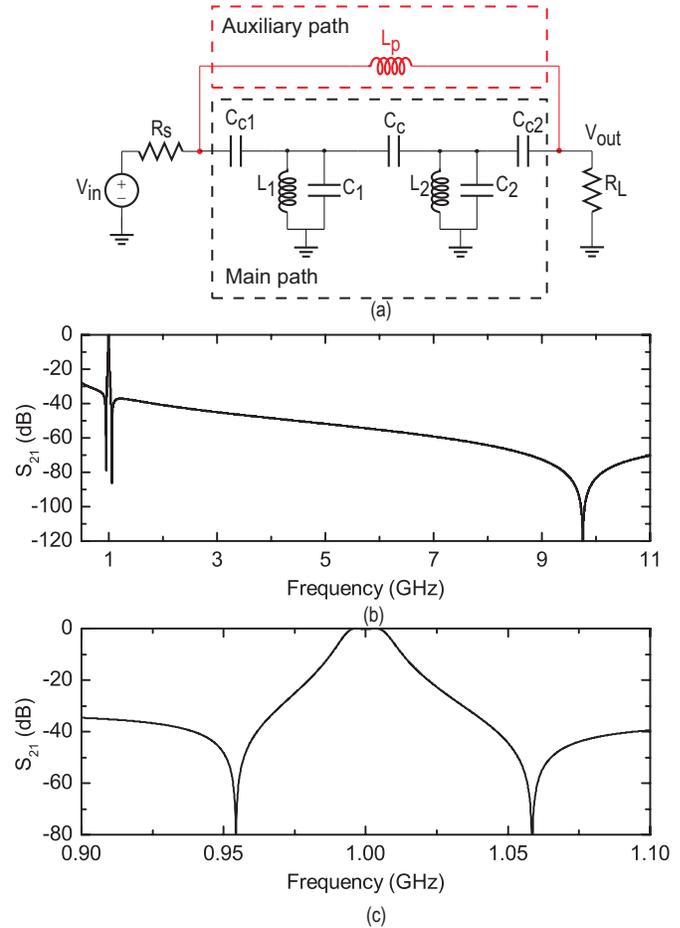


Fig. 1. (a) Proposed filter to create transmission zeros.(b) Simulated response for $L_1=12$ nH, $C_{c1} = C_{c2}=0.246$ pF, $C_c=0.024$ pF and $L_p=800$ nH. The three finite transmission zeros are at 954 MHz, 1.06 GHz and 9.76 GHz. (c) Zoomed in view of fig. (b) to show close-in notches.

end LNA used in [3] might be desensitized in presence of high power blockers if the LNA is not highly linear. Due to the use of smaller supply voltage in modern CMOS process, achieving high linearity is challenging and a passive front end filter may still be preferred [4].

In this paper a low power tunable bandpass filter with integrated adaptive notch is presented handle large out-of-band dynamic blockers. In section II, the design of the proposed bandpass filter is demonstrated. Section III describes the real implementation, section IV reports the filter performance and section V concludes the paper.

II. DESIGN METHODOLOGY

The proposed filter consists of a second-order coupled resonator bandpass (BP) filter with capacitive coupling in parallel with a feedback inductor as shown in Fig. 1(a). The inductor is introduced to create transmission zeros on both sides of the passband. A combination of capacitive and inductive coupling among bandpass resonators along with a feedback capacitor is independently proposed in [5] to create dual notches close to the passband. However, this topology is difficult to tune due to the use of inductors in the main path as the tuning of on-chip inductor is limited.

The overall admittance matrix for the proposed filter schematic will be the sum of the main path and the auxiliary path. In such a case, the overall admittance matrix of the overall filter is of the form

$$Y = \begin{pmatrix} \frac{1}{sL_p} + y'_{11} & -\frac{1}{sL_p} + y'_{12} \\ -\frac{1}{sL_p} + y'_{21} & \frac{1}{sL_p} + y'_{22} \end{pmatrix}$$

where $s = j\omega$ and $y'_{11}, y'_{12}, y'_{21}, y'_{22}$ are the elements of the admittance matrix for the coupled resonator filter without the feedback inductor.

Using this admittance matrix, the location of the finite transmission zeros can be obtained by solving the following equation:

$$-\frac{1}{sL_p} + y'_{12} = 0 \quad (1)$$

The element y'_{12} can be found by performing the nodal analysis on the main path

$$y'_{12} = -\frac{sC_c C_{c1} C_{c2}}{\left(C'_1 + \frac{1}{s^2 L_1}\right) \left(C'_2 + \frac{1}{s^2 L_2}\right) - C_c^2} \quad (2)$$

where $C'_1 = C_1 + C_{c1} + C_c$ and $C'_2 = C_2 + C_{c2} + C_c$.

Now, by substituting (2) to (1) and rewriting it as

$$s^6 L_1 L_2 L_p C_c C_{c1} C_{c2} + s^4 L_1 L_2 K + s^2 (L_1 C'_1 + L_2 C'_2) + 1 = 0, \quad (3)$$

where $K = C'_1 C'_2 - C_c^2$.

A sixth-order polynomial in s is obtained, which means there are three finite transmission zeros and the locations of the three finite transmission zeros will be the three positive roots of the polynomial. It is also possible to solve the equation graphically [5]. Fig. 1(b) shows three different real transmission zeros for $L_1=12$ nH, $C_1 = 1.842$ pF, $C_{c1}=0.246$ pF, $C_c=0.024$ pF and $L_p=800$ nH. The simulated notch frequencies are at 954 MHz, 1.06 GHz and 9.76 GHz. whereas (3) predicts the notch frequencies at 953.7 MHz, 1.059 GHz and 9.637 GHz.

Fig. 2(a) shows the notch depth with respect to the quality factor Q of the inductor. The filter shows a minimum of 40 dB rejection at the notch frequency with Q as low as 5 which is a feasible value for on-chip and off-chip inductor implementations.

The primary idea of the proposed filter is to replace the two bandpass resonators with their N-path counterparts [2]. In a N-path filter the center frequency of the tank is determined by

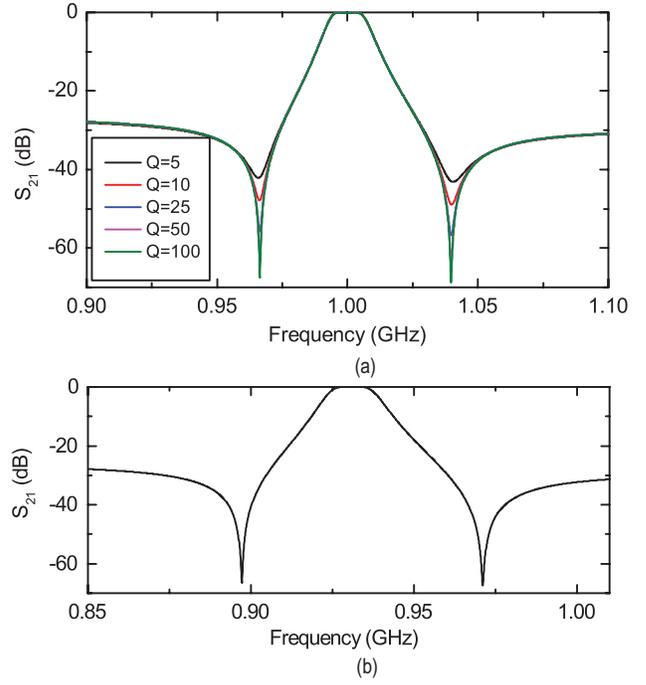


Fig. 2. (a) The effect of inductor Q on notch creation. The feedback inductor was specified as 400 nH in the simulation. (b) The filter response with the resonators resonate at 1 GHz. The center frequency of the overall filter is shifted to lower frequency.

the clock instead of the baseband capacitor. Therefore, the center frequency of the N-path filter can be widely tuned. Fig. 2(b) shows the filter response for $L_1=12$ nH, $C_1 = 2.11$ pF, $C_{c1}=0.297$ pF, $C_c=0.0297$ pF and $L_p=400$ nH. The resonant frequency of each resonant tank is 1 GHz (previously it was 1.07 GHz), however the center frequency of the overall filter is shifted to approximately 930 MHz. However, the center frequency shifting is acceptable as the proposed filter is tunable.

III. PROPOSED FILTER DESIGN

A. Circuit Implementation

The complete schematic of the proposed filter is shown in Fig. 3. The bandpass resonators are implemented with R-C configuration of N-path filters. The feedback inductor shown

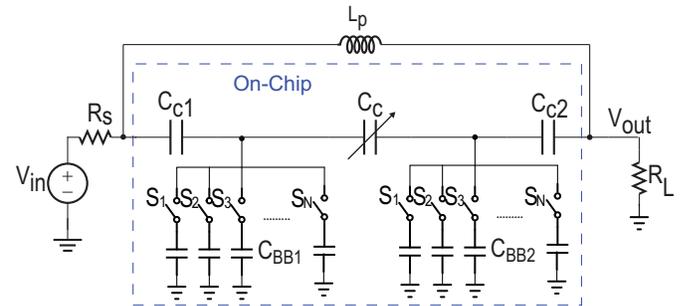


Fig. 3. N-path implementation of the proposed filter. Inductor L_p is an off-chip inductor.

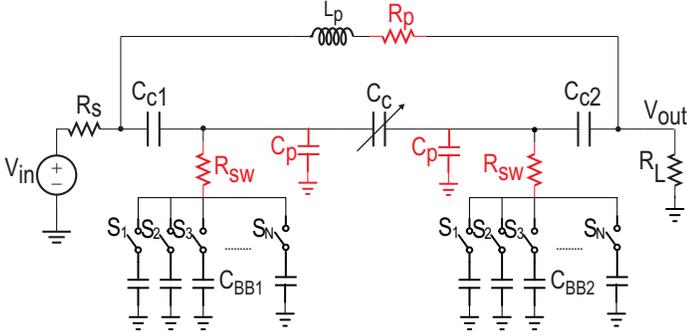


Fig. 4. The parasitic capacitance and resistance at different nodes on the proposed filter.

in the previous simulation is extremely big even for off-chip implementation. Therefore, it is necessary to reduce the inductor size. On the other hand, if the baseband capacitor size is small, then it is dominated by the parasitic capacitance. So, it is necessary to increase the baseband capacitance. According to (3), the transmission zeroes location are dependent on the baseband capacitor as well as the feedback inductor. The transistor sizes used as a switches in the bandpass sections are ($W/L = 80 \mu\text{m}/60 \text{ nm}$). The baseband capacitors used in the bandpass sections are 20 pF, $C_{c1} = 6 \text{ pF}$, $C_c = 3 \text{ pF}$ and $L_p = 40 \text{ nH}$ for LO frequency of 1 GHz. The calculated transmission zero locations from (3) are 841.5 MHz, 1.06 GHz and 4.25 GHz.

A master clock (CLK) at 4 times the switching frequency is applied from off-chip. A D-flip-flop (D-FF) based divider divides the input clock by 4, while an AND gate between the divide by 4 outputs generates a 25% duty cycle clock. A shift register implemented with transmission gate flip-flops produces 4-phase clocks to drive the switches in bandpass resonators. Metal-insulator-metal (MIM) capacitors are used in the proposed implementation, which contains parasitic capacitance of approximately 1% of the total capacitance on each side. In next section, we will describe the parasitic capacitance effect on the filter performance.

B. Parasitic Effects

Fig. 4 shows the proposed schematic with parasitic capacitance and switch resistance. A series resistance is also added with the feedback inductor to represent the Q of the inductor. The switches have a non-zero switch resistance R_{sw} which can modify the transfer function of the filter. R_{sw} reduces the Q of baseband capacitors as well as the Q of the overall filter. It also modifies the pole locations of the filter [6]. As a result, it may not be possible to generate symmetric transmission zeros on both sides of the passband due to amplitude and phase mismatch. On the other hand, the parasitic capacitance for the bandpass resonators include contributions from the top side of the switches, RF signal routing line and top plate of MIM capacitors. The parasitic capacitance lowers the center frequency of the filter as well as introduces insertion loss [7]. Fig. 5 shows the filter response of Fig. 1(a) by adding parasitic

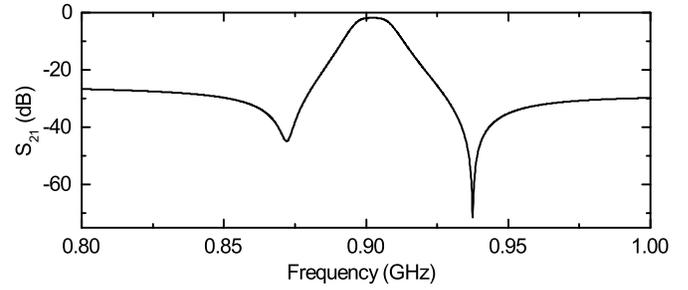


Fig. 5. The notch becomes asymmetric by adding the parasitic capacitance and resistance. $L_1 = 12 \text{ nH}$, $C_1 = 2.11 \text{ pF}$, $C_{c1} = 0.297 \text{ pF}$, $C_c = 0.0297 \text{ pF}$, $C_p = 0.157 \text{ pF}$ and $L_p = 400 \text{ nH}$, $R_p = 120 \Omega$

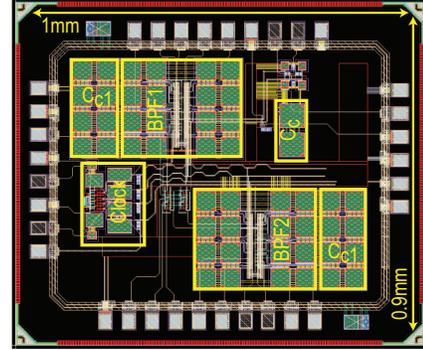


Fig. 6. The layout of the proposed filter. The total area including bondpad is 0.9 mm^2 .

capacitance $C_p = 0.157 \text{ pF}$ after each bandpass resonators. The inductor Q is specified as 20. The transmission zero at the left side is much shallower than the right one due to the asymmetric response of the coupled bandpass filter with parasitics.

IV. FILTER PERFORMANCE

The proposed filter has been designed in a 65 nm CMOS process. The layout of the proposed filter is shown in Fig. 6. The total area of the proposed filter including bonding pads is 0.9 mm^2 . Coilcraft 1206CS-270 can be used as the feedback

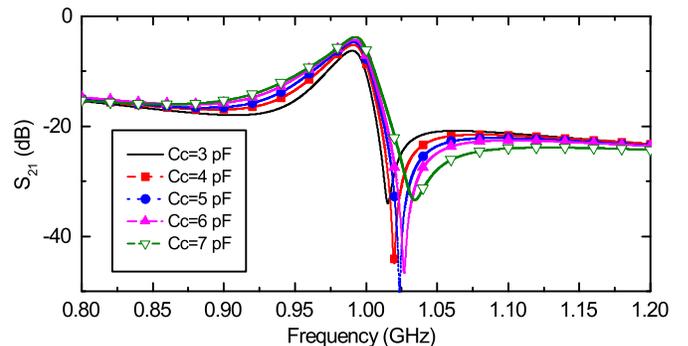


Fig. 7. The notch frequency can be shifted by changing the coupling capacitor C_c .

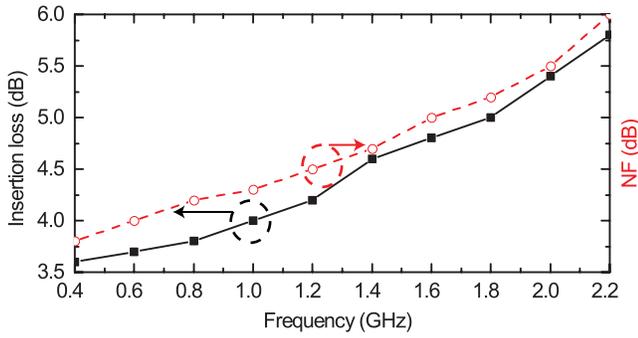


Fig. 8. The simulated insertion loss and group delay of the filter.

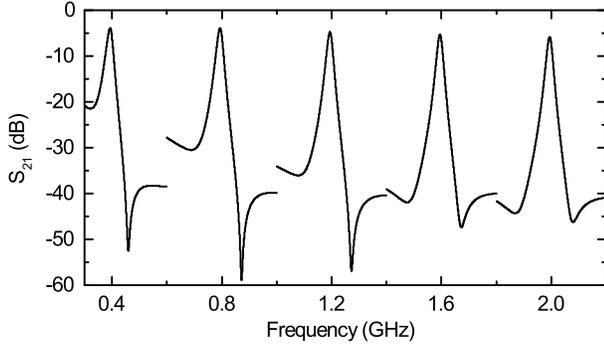


Fig. 9. The simulated transfer function of the filter shown at every 400 MHz over the frequency range from 0.4 GHz to 2 GHz.

inductor with Q of 120 at 1 GHz.

Fig. 7 shows the tunability of the notch by changing the coupling capacitor with post layout simulation. The notch frequency is tunable by 20 MHz. The filter shows one deep notch on the right side, while the left side notch gets shallower due to mismatch and parasitics. Due to the high attenuation at a particular frequency and the tunability, the proposed filter can significantly block the strong blocker/transmitter in the receive band.

The noise figure (NF) of the filter along with the insertion loss is shown in Fig. 8. The filter has 3.6~5.8 dB insertion loss in the whole tuning range. The loss of the filter increases at higher frequency. The NF of the proposed filter is 3.8–6 dB. The proposed filter is tunable from 400 MHz to 2.2 GHz. The transfer function over the whole tuning range is shown in Fig. 9. The 3-dB BW of the filter is 14.4 MHz–15.6 MHz with power consumption of 12.4–42 mW. Two-tone IIP3 and compression measurements are shown in Fig. 10. The simulated out-of-band IIP3 (OOB) of +23.5 dBm is obtained at Δf of 40 MHz and f_{io} of 1 GHz. The filter is compared with state-of-the-art integrated filters in Table I.

V. CONCLUSION

A low power all passive tunable bandpass filter with adjustable transmission zero is presented. The filter can handle large out-of-band blockers at a particular offset by creating a notch at that frequency. Due to the tunability of the notch, the

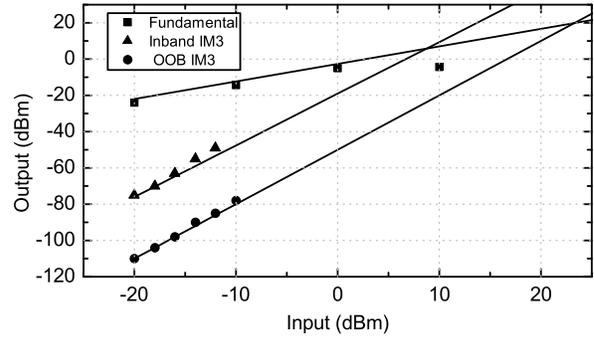


Fig. 10. The simulated out-of-band linearity of the filter.

TABLE I
COMPARISON TABLE

	Chen [4]	Naimul [2]	Luo [3]	This work
Circuit Type	Filter	Filter	LNA	Filter
CMOS Tech.	65 nm	65 nm	32 nm SOI	65 nm
Topology	Passive SC	Active SC	Active SC + LNA	Passive SC
Frequency range [GHz]	0.5–1.1	0.4–1.4	0.4–6	0.4–2.2
Gain [dB]	-4.6~5.2	17	10	-3.6~5.8
# of notches	0	1	2	1
BW [MHz]	30	6.4	15	14.4–15.6
NF [dB]	2.6	3.8–4.7	3.6–4.9	3.8–6
Blocker P1dB [dBm]	11	4	17	8.5
IIP3 (OOB) [dBm]	26	12–14	36	23.5
Power [mW]	15–25	36.4–56	81–209	12.4–42 ¹

¹Power is consumed in the clock path. Signal path is completely passive

proposed filter is more robust compared with other state-of-the-art front end filters and duplexers. The filter is also tunable over a wide tuning range while maintaining constant insertion loss.

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