Low-loss and Broadband G-Band Dielectric Interconnect for Chip-to-Chip Communication

Bo Yu, Yuhao Liu, Yu Ye, Xiaoguang “Leo” Liu, and Qun Jane Gu

Abstract—This paper presents a novel dielectric waveguide based G-band interconnect. By using a new transition of microstrip line to dielectric waveguide, the interconnect achieves low insertion loss and wide bandwidth. The measured minimum insertion loss is 4.9 dB with 9.7 GHz 1-dB bandwidth. Besides, the structure is based on standard micromachined processing and easy to integrate with conventional packaging.

Index Terms—Deep reactive ion etching, dielectric waveguide, G-band, interconnect, micromachined, sub-THz, transition.

I. INTRODUCTION

FUELED by the demand of high data rate and low loss chip-to-chip communication, the interconnect gap have been a challenging issue over decades [1], [2]. Sub-THz/THz interconnect, using the spectrum sandwiched between optical and microwave frequencies, holds high potentials to fill the interconnect gap with wide bandwidth density and high energy efficiency by leveraging advantages of both optical and electrical interconnect approaches: low loss quasi-optical channels as well as advanced high speed semiconductor devices [3].

In general, the interconnect can be classified into three types, transmission line, including microstrip line (MSL), coplanar waveguide (CPW), grounded CPW, etc., metallic waveguides (MWG), and dielectric waveguide (DWG). The key aspects for inter-chip interconnect include low loss, wide bandwidth, reliable and compatible fabrication with silicon processes. The DWGs with low loss dielectric material have much less losses than transmission lines and MWGs since the conduction loss is avoided [4]–[7]. The loss for the CMOS transmission line is about 1 dB/mm at 100 GHz and 2 dB/mm at 150 GHz and increases fast with frequency [8], [9]. Moreover, from the process-compatible point of view, the DWGs are easier to fabricate and potentially compatible with integrated silicon circuits compared with MWGs. The comparison table is listed in Table I.

In this work, we propose a G-band (140-220 GHz) interconnect by combining the MSL and DWG. Compared with other interconnect, the proposed interconnect is low loss, wide bandwidth, fully micromachined, and easy to integrate with conventional packaging. The channel design methodology can be readily applied to higher frequencies in the THz range.

II. INTERCONNECT DESIGN

Fig. 1(a) and (b) shows the configuration of the proposed G-band interconnect channel with two back-to-back transitions between the DWG and the MSL. Each transition consists of a tapered DWG and MSL to transit the electromagnetic wave smoothly. These two tapers overlap each other without gap. The 50-Ω MSL is designed on a 100-µm quartz substrate with the metal width of 218 µm. The straight DWG with 450-µm width and 500-µm height is designed according to [3]. The magnitude of E-field distribution of the transition is plotted in Fig. 1(c), which indicates the smooth mode transition between the MSL and the DWG.

The cross-section of simulated E-field distributions for the transition are illustrated in Fig. 2. The mode gradually transitions from the quasi-TEM in the MSL as shown in Fig. 2(b), to the hybrid mode in transition as shown in Fig. 2(c) and (d), and then to the E_{y11} mode in the DWG as shown in Fig. 2(e). The magnitude of E-field distribution of the transition is plotted in Fig. 1(c), which indicates the smooth mode transition between the MSL and the DWG.

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Table I

Comparison among Different Technologies of Interconnects

<table>
<thead>
<tr>
<th>Design</th>
<th>Type</th>
<th>Loss (dB/mm)</th>
<th>Planar Process Integration</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>DWG</td>
<td>0.058 @ 500 GHz</td>
<td>Hard</td>
</tr>
<tr>
<td>[6]</td>
<td>MWG</td>
<td>0.05 @ 105 GHz</td>
<td>Hard</td>
</tr>
<tr>
<td>[7]</td>
<td>MWG</td>
<td>0.15 @ 600 GHz</td>
<td>Hard</td>
</tr>
<tr>
<td>[8]</td>
<td>MSL</td>
<td>2 @ 150 GHz</td>
<td>Easy</td>
</tr>
<tr>
<td>This work</td>
<td>DWG</td>
<td>0.014 @ 140-190 GHz</td>
<td>Easy</td>
</tr>
</tbody>
</table>

*Without the transition

Fig. 1. (a) Top view of the G-band interconnect, (b) perspective view of the transition, (c) the magnitude of E-field distribution of the transition at 160 GHz.

Fig. 2. (a) Sub-THz Interconnect, (b) Transition, (c) Quartz, (d) HR Silicon, (e) MSL, Port1, Port2.
and 120 Ω with the 20-µm width. For the DWG, the real part of the impedance increases and then decreases with the increase of the DWG width because the dominant mode is changed from the evanescent mode to the $E_{11}$. It is 45 Ω when the DWG width is 30 µm and 133 Ω when the DWG width is 450 µm.

To describe the matching performance, the theory of small reflections is used to analyze the reflection coefficient response as a function of the impedance taper versus position [10]. The incremental reflection coefficient from impedance step at $x$ axis is given by

$$\Delta \Gamma = \frac{(Z + \Delta Z) - Z}{(Z + \Delta Z) + Z} \approx \Delta Z \frac{2Z}{Z^2} \quad (1)$$

where $Z$ is characteristic impedance, $\Delta Z$ is the impedance change step. Therefore, the total reflection coefficient is derived as

$$\Gamma(2\beta l) = \frac{1}{2} \int_{x=0}^l [e^{-j2\beta x} \frac{d}{dx} \ln(Z(x))] dx \quad (2)$$

where $x$ is the taper position, $l$ is the taper length, and $\beta$ is the propagation constant. According to (2), the reflection coefficient of the transition with the various taper length is calculated compared with the simulated results in Fig. 4. The difference between the calculation and the simulation is due to the slight impedance mismatch between the MSL and the DWG at 160 GHz. As shown in Fig. 4, the optimized taper length is about 1500 µm. The minimum insertion loss for the transition is 0.44 dB with 51.9-GHz 1-dB bandwidth as shown in Fig. 5.

The complete interconnect consists of a 10-mm straight DWG with two back-to-back transitions in Fig. 6. Fig. 6(a) shows an interconnect with a separate substrate, and Fig. 6(b) shows the one with a joined substrate and backside metal. The minimum insertion loss is 1.55 dB with 38.9 GHz 1-dB bandwidth for the separate substrate and is 0.96 dB with 42.5 GHz 1-dB bandwidth for the joined substrate as shown in Fig. 6(c). To simplify the fabrication processing, the design presented in this paper chooses the joined substrate.

### III. EXPERIMENTAL AND DISCUSSION

The fabrication processes of the interconnect with fabricated photos are summarized in Fig. 7. A 500-µm thick high resistivity (HR) silicon wafer ($\rho = 10000 \ \Omega \cdot cm$, $\varepsilon_r = 11.9$, $\tan \delta = 0.001$) is first patterned with a thick (~12 µm) photoresist (AZ9260) to define the waveguide geometries. Then, the HR silicon wafer is attached to a carrier substrate and etched through in a DRIE process. The coupling structure is fabricated on a 100-µm quartz substrate ($\varepsilon_r = 3.78$). The coupling structure is patterned with a Ti/Au ($\sigma = 4.1 \times 10^7 \ S/m$) thin film of thickness 20/200 nm by a lift-off process. Both DWG and MSL photos are shown in Fig. 7. The measurement setup consists of an Agilent network analyzer (PNA-X N5247A), a pair of Virginia Diodes fre-
frequency extension modules (VDI WR5.1-VNAX), WR-5 (140-220 GHz) S-band waveguides, and a pair of WR-5 probes. The SOLT (Short, Open, Load, Thru) calibration method is employed to set the reference plane at the probe tip. Therefore, the measured interconnect path includes the interconnect, two 1.4-mm MSLs, and two CPW-to-MSL transitions. The alignment is completed by using alignment marks on the each side of coupling structure of designed on the quartz substrate.

Fig. 8 presents the simulated and measured S-parameters of the interconnect. The measured minimum insertion loss for the 10-mm interconnect is 4.9 dB with 9.7-GHz 1-dB bandwidth. The results can be further improved by reducing the gap and the assembly offsets between the MSL and DWG. This new interconnect is based on standard micromachined processing method, making it compatible with standard packaging method. Besides, it can be easily extendable to THz frequencies due to the low insertion loss and no conduction loss with HR silicon DWG.

**REFERENCES**


