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Application Note:

The main parts I focused on for this project are the main chip schematic layout drawing, review the PCB layout, debugging the systems, and the low pass filter design.

For most of the chips such as VGA, VCO, and the RF amplifiers layouts, first, I need to read the datasheet for each of them. Most importantly, since some parts of our design are different than some default design of those datasheet. I need to make sure all the resistances and lines changes I made are correct for our own design.

For VGA, since we are using the auto detective (AGC), we pick a chip that works from low frequency to 10kHz. I made the schematic for our AGC cleaner to build so therefore we can minimize the size of our PCB for lighter weight can cleaner.

For VCO, the default schematic was exactly what we want.

For RF amplifiers, I need to connect 3 RF amplifiers for the receiving stage of the PCB for combining of flexible 50 dB depends on the distance of the object.

For PCB layout review, I need to check line by line with the chip schematic layout I had before and check if the components are correct from the layout Jeon made. Secondly, I need to make sure the lines between each component are fairly separately so there will be no interference during either our test work or manufactured.

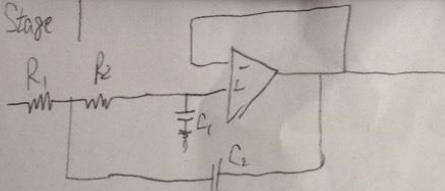
For debugging the systems for each chips whether they functioning or not individually, we use function generator and the operating voltage to operate only that chip and use oscilloscope for the result compare. Since for each component we have the corresponding output node for testing, it is fairly easy to see if the chip is correctly soldering for work.

For designing the low pass filter, we use the WEBENCH design program online to design a 4th order Butterworth Low pass filter. In order to see if the design make sure, I also made hand calculation about the low pass filter and it is really accurate for our design need.

Since we want the first stage to stay gain 1, and 4.5 gain for second stage, this is not the normal way to design the Butterworth. However, due to the voltage problem from our power supplying, there is no other way to do it.

It was hard to find the exact same values of resistors or capacitors we want from the design. Therefore, I need to make some calculations and replace them with some other values in order to make the values as close as possible from the speciation we want for our design

Stage 1



$$f_c = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

$$= \frac{1}{2\pi \sqrt{910 \times 16200 \times 1.5 \times 10^{-9} \times 910 \times 10^{-12}}}$$

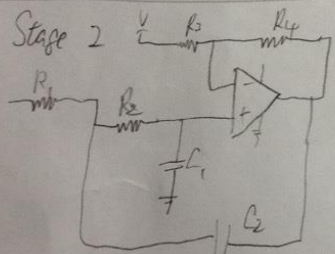
$$= \frac{1}{2\pi \sqrt{1.46909 \times 10^5}}$$

$$= 10833 \text{ Hz}$$

$R_1 = 910 \text{ } \Omega$
 $R_2 = 16.2 \text{ k} \Omega$
 $C_1 = 910 \text{ pF}$
 $C_2 = 1.5 \text{ nF}$

$$Gain = 1 + \frac{R_A}{R_B} = 1 + \frac{0}{0} = 1 \text{ V/V}$$

Stage 2



$$f_c = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

$$= \frac{1}{2\pi \sqrt{35700 \times 8660 \times 910 \times 10^{-12} \times 210 \times 10^{-12}}}$$

$$= 18260.9926$$

$$\approx 18261 \text{ Hz}$$

$R_1 = 35.7 \text{ k} \Omega$
 $R_2 = 8.66 \text{ k} \Omega$
 $R_3 = 2.26 \text{ k} \Omega$
 $R_4 = 1.87 \text{ k} \Omega$
 $C_1 = 910 \text{ pF}$
 $C_2 = 210 \text{ pF}$

$$Gain = 1 + \frac{R_4}{R_3} = 1 + \frac{1.87}{2.26} = 4.482 \text{ V/V}$$